UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,901	02/06/2004	Woo-yeong Cho	SAM-0519	8597

7590 09/20/2005

Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,901	CHO ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-55 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-55 is/are rejected.

7)☒ Claim(s) 13,14 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 July 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date (1) 2/6/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Search History.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 6, 2004, the Foreign Priority filed on February 6, 2004, and the Information Disclosure Statement filed on February 6, 2004.

2. Claims 1-55 are pending in the case. Claims 1 and 27 are independent claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received in Application.

Claim Objections

4. Claims 13 and 14 are objected to because of the following informalities: Claim 13 and claim 14 are out of order. It is suggested to move claim 13 above claim 14.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-46, and 49-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al. U.S. Patent 6,813,177B2 in view of Tang et al. U.S. Patent 6,222,771B1 as supported by Ooishi U.S. Patent 6,873,561B2.**

Regarding independent claim 27, Lowrey et al. '177B2 shows a semiconductor memory device (Fig. 2 [115]) that sends programming signals to the memory (column 4, lines 49-51). The programming signal can be a set pulse or a reset pulse. A read device may be used to verify the state of the memory cells during programming (column 4, lines 53-55). After a programming signal is applied to the memory cells, the resistance of the phase change device may be read to determine if the memory cell was programmed to the desired state. This process of applying a programming signal and reading or verifying the resistance of the memory cell may be referred to as a feedback approach for programming the memory cells (column 5, lines 11-18). Applying this programming signal, with same duration and same amplitude, until the resistance in the memory cell is within adequate ranges may be repeated (column 5, line 45-49). Lowrey et al. '177B2 lacks the detection of the memory state simultaneously to the application of the programming pulse.

Tang et al. '771B1 shows a semiconductor memory device (Fig. 1 [10]) comprising a detecting circuit (Fig. 2 [210]) for detecting the state of the memory device (Fig. 2 [MC]). Tang et al. '771B1 also shows a controller (Fig. 2 [210]), same as detection circuit, that removes a programming signal when the memory is detected to be in a desired state so that the duration of the programming pulse is controlled based on the state of the memory. The signal controlling the memory (Fig. 2 [MC]) is enabled or disabled by a switch (Fig. 2 [212]) that is dependent on the output of a comparison circuit (Fig. 2 [218]) which is dependent on the state of the memory device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Tang et al. '771B1, with respect to applying a programming pulse to a memory device while detecting the state of the memory, to implement state dependent circuitry into the memory device of Lowrey et al. '177B2 such that the programming signals will be applied to the memory device continuously until the desired memory state is achieved for the purpose of concurrently programming a memory cell while verifying the voltage across that memory cell (Tang et al. '771B1 column 5, lines 30-32). Further motivation to perform the above stated modification are evidented by the fact that both Lowrey et al. '177B2 and Tang et al. '771B2 are from the same field of endeavor such as being classified under U.S. Cl. 365 and comprising memory cells and sensing amplifiers.

As per **claim 1**, it encompasses the same scope of invention as to that of claim 27 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claims 28-30, Lowrey et al. '177B2 shows that the reset state is the amorphous state and that the set state is the crystalline state (column 3, lines 47-49).

As per **claims 2-4**, they encompass the same scope of invention as to that of claims 28-30 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding dependent claims 31-32, Lowrey et al. '177B2 shows a detector (Fig. 6 [150]) that detects a read voltage of a device (Fig. 6 [140]). The

read voltage is indicative of the resistance of memory cell (Fig. 6 [140]), and therefore, may be used to indicate the state of memory cell (column 12, lines 63-65). The detected resistance, as based off of the read voltage, is the resistance of the memory cell (Fig. 6 [140]).

As per **claims 5-6**, they encompass the same scope of invention as to that of claims 31-32 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding dependent claim 7, Lowrey et al. '177B2 shows the crystalline state is of a low resistance and the amorphous state is of a high resistance (column 3, lines 36-37).

Regarding dependent claims 33-35, Lowrey et al. '177B2 shows a detector (Fig. 6 [150]) detecting a voltage from the column line (Fig. 6 [130]). This column line is a bit line (see Fig. 2). The detector circuit (Fig. 6 [150]) comprises a sense amplifier (Fig.6 [713]).

As per **claim 8**, it encompasses the same scope of invention as to that of claim 33 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claims 37-39, Lowrey et al. '177B2 shows a timing device (Fig. 2 [170]), or controller, that generates timing signals to assist with read and write operations (column 4, lines 48-49). Lowrey et al. '177B2 is silent with respect to a write enable signal; however, it is well known in the art that a memory comprises write enable signals that allow for programming via programming lines when a write enable line is asserted. Lowrey et al. '177B2

omits the description of this feature because it is understood by those skilled in the art that the claimed subject matter may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the claimed subject matter (Lowrey et al. '177B2 column 2, lines 1-5). Such write enable feature that is omitted in Lowrey et al. 177B2 is shown in Ooishi '561B2 (Ooishi '561B2 column 18, lines 1-2).

As per **claims 9-11**, they encompass the same scope of invention as to that of claims 37-39 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding dependent claims 40-45, and in addition to the claims covered above, Lowrey et al. '177B2 shows a set pulse is applied until the memory is in a desired low resistive state, or crystalline state. The resistive state of the memory is determined by the voltage across the memory cell as compared to a reference voltage (Fig. 6 [REF3]). A lower voltage indicates that the cell is in a relatively low resistance state (column 4, lines 65-66; column 5, lines 1-2). When the comparator determines that the resisitivity of the memory cell is low (C3 = "L"; see column 13 truth table), the state is determined to be the crystalline, or set, state. The reference voltage (Fig. 6 [REF3]) is a set programming voltage. When the memory is applied the set pulse to place the phase change memory cell in the set state, if the bit line voltage is equal to or below the reference voltage, or set programming voltage, then the set pulse is removed.

As per **claims 12, and 14-18**, they encompass the same scope of invention as to that of claims 40-45 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding dependent claim 36, Lowrey et al. '177B2 shows that a set pulse is applied until the memory is in a desired low resistive state, or crystalline state. The resistive state of the memory is determined by the voltage across the memory cell as compared to a reference voltage (Fig. 6 [REF3]). A lower voltage indicates that the cell is in a relatively low resistance state (column 4, lines 65-66; column 5, lines 1-2). When the comparator determines that the resisitivity of the memory cell is low (C3 = "L"; see column 13 truth table), the state is determined to be the crystalline, or set, state. The reference voltage (Fig. 6 [REF3]) is a set programming voltage.

As per **claim 13**, it encompasses the same scope of invention as to that of claim 36 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 46, Lowrey et al. '177B2 shows a signal generator device (Fig. 2 [160]) that applies the set pulse to the bit lines. By Ohm's Law, current and resistance are directly related to voltage; i.e., a signal carrying a voltage applied to a line will invariably also carry a current. Thus, applying a voltage to a bit line will also result the application of a current to the same bit line.

As per **claim 19**, it encompasses the same scope of invention as to that of claim 46 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claims 49, Lowrey et al. '177B2 shows a detector (Fig. 6 [150]) that detects a read voltage from the column line, or bitline (Fig. 6 [130]). The read voltage is indicative of the resistance of memory cell (Fig. 6 [140]), and therefore, may be used to indicate the state of memory cell (column 12, lines 63-65). By Ohm's Law, current and resistance are directly related to voltage; i.e., a signal carrying a voltage applied to a line will invariably also carry a current. Thus, applying a voltage to a bit line will also result the application of a current to the same bit line; or, the voltage of the bit line is detected while a current is applied to the line.

As per **claim 20**, it encompasses the same scope of invention as to that of claim 49 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claims 50, Lowrey et al. '177B2 shows that the timing device (Fig. 2 [170]), or controller, that generates timing signals to assist with read and write operations (column 4, lines 48-49). The signal generator (Fig. 2 [160]), or driver, applies programming pulses to the column lines, or bit lines, of the memory device.

As per **claim 21**, it encompasses the same scope of invention as to that of claim 50 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claims 51-53, Lowrey et al. '177B2 shows that phase change alloys are used in this memory device. A chalcogenide containing one or more elements from Column VI of the periodic table may be used in the memory device. The memory device may comprise GeSbTe alloys (column 3, lines 21-25).

As per **claims 22-24**, they encompass the same scope of invention as to that of claims 51-53 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Regarding dependent claim 54, Lowrey et al. '177B2 shows that the reset state, or amorphous state, requires a higher current than the set state, or crystalline state (Fig. 5 and column 11, lines 39-41).

As per **claim 25**, it encompasses the same scope of invention as to that of claim 54 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 55, Lowrey et al. '177B2 shows that the fall time, or pulse width, of the programming signal applied to a phase change material may be increased to reduce the resistance of the phase change material, and conversely, the fall time of the programming signal may be decreased to increase the resistance of the phase change material (column 9, lines 5-10). Thus, the pulse width of the signal used to place the phase change material in a high resistive state, or amorphous state, is narrower than the pulse width of a signal used to place the phase change material in a low resistive state,

or crystalline state; where the amorphous state is resultant of a reset pulse and the crystalline state is resultant of a set pulse.

As per **claim 26**, it encompasses the same scope of invention as to that of claim 55 except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

7. **Claims 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al. U.S. Patent 6,813,177B2 in view of Tang et al. U.S. Patent 6,222,771B1 in further view of Lowrey et al. U.S. Patent 6,608,773B2.**

Regarding dependent claims 47-48, Lowrey et al. '177B2 shows that the timing device (Fig. 2 [170]), or controller, that generates timing signals to assist with read and write operations (column 4, lines 48-49). The signal generator (Fig. 2 [160]), or driver, applies programming pulses to the column lines, or bit lines. Lowrey et al. '177B2 is silent with respect to the set enable signal and reset enable signal. Lowrey et al. '177B2 also lacks the detection of the memory state simultaneously to the application of the programming pulse.

Lowrey et al. 773B2 shows the set enable feature (Fig. 8 [Q_{SET}]) and the reset enable feature (Fig. 8 [Q_{RESET}]).

Tang et al. '771B1 shows a semiconductor memory device (Fig. 1 [10]) comprising a detecting circuit (Fig. 2 [210]) for detecting the state of the memory device (Fig. 2 [MC]). Tang et al. '771B1 also shows a controller (Fig. 2 [210]), same as detection circuit, that removes a programming signal when the memory is detected to be in a desired state so that the duration of the programming pulse

is controlled based on the state of the memory. The signal controlling the memory (Fig. 2 [MC]) is enabled or disabled by a switch (Fig. 2 [212]) that is dependent on the output of a comparison circuit (Fig. 2 [218]) which is dependent on the state of the memory device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Tang et al. '771B1, with respect to applying a programming pulse to a memory device while detecting the state of the memory, to implement state dependent circuitry into the memory device of Lowrey et al. '177B2 such that the programming signals will be applied to the memory device continuously until the desired memory state is achieved for the purpose of concurrently programming a memory cell while verifying the voltage across that memory cell (Tang et al. '771B1 column 5, lines 30-32). Additionally, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Lowrey et al. '773B2 to implementing a set enable feature (Lowrey et al. '773B2 Fig. 8 [Q_{SET}]) and a reset enable feature (Lowrey et al. '773B2 Fig. 8 [Q_{RESET}]) in between the timing device (Lowrey et al. '177B2 Fig. 2 [170]) and the signal generator (Lowrey et al. '177B2 Fig. 2 [160]) such that the timing signals are used as enable signals to selectively activate the set pulse or reset pulse to the bit line of the memory device until the desired memory state is achieved for the purpose of concurrently programming a memory cell while verifying the voltage across that memory cell (Tang et al. '771B1 column 5, lines 30-32). Further motivation to perform the above stated modification are evidenced by the fact that Lowrey et al. '177B2, Tang et al.

'771B2, and Lowrey et al. '773B2 are from the same field of endeavor such as being classified under U.S. Cl. 365 and comprising memory cells and sensing amplifiers.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hwang et al. U.S. Patent Application 2005/0117387A1, Lee et al. US Patent 6,862,214B2, Lowrey et al. U.S. Patent 6,545,907B1, and Lowrey et al. U.S. Patent 6,570,784B2. All of these references shows phase change memory configurations.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

ANH PHUNG
PRIMARY EXAMINER